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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,219	JUAN ET AL.	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on th cover sh et with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-14,19-24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 10-14, 19-24, and 26-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5, 10-14, 19-24, and 26-27 have been considered. Claims 1, 10, 14, 19, 24, and 26 have been amended as per Applicant's request. Claims 6-9, 15-18, and 25 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Extension of Time for 1 Month as received on 15 November 2004.

Claim Objections

3. Claim 10 is objected to because of the following informalities: Please correct claim 10 from "if the store is poisoned, sets a poison value that indicates through a store set dependence that that the store is poisoned" to -- if the store is poisoned, sets a poison value that indicates through a store set dependence that ~~that~~ the store is poisoned--. The correction is indicated with a strikethrough. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-5, 10-14, and 19-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims

1, 10, and 19 recite the limitation "applies said poison value through the store set dependence to subsequent load/store order violation occurrences" implying that all loads subsequent to the poisoned store have the poison value applied to it. However, the specification only discloses propagating the poison value to subsequent dependent loads.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-5, 10-14, and 19-23 are recites the limitation " applies said poison value through the store set dependence to subsequent load/store order violation occurrences " in the claim but not in the specification. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-5, 10-14, 19-24, and 26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Merchant et al., U.S. Patent No. 6,665,792.

10. Regarding claims 1, 10 and 19, taking claim 10 as exemplary, Merchant has taught a computer system, comprising:

a. A microprocessor (100 of Fig. 1) comprising a store set identifier table (see column 6, lines 4-16 and 40-49 and Figures 2 and 3),

b. An input device coupled to said microprocessor (IQ, 112 of Fig. 1),

c. Memory coupled to said microprocessor, said memory containing executable instructions (104 of Fig. 1),

d. Wherein said microprocessor:

i. Fetches instructions from said memory (see Col.3 line 54 – Col.4 line 8), certain fetched instructions being load instructions (loads) and causing load operations, and other fetched instructions being store instructions (stores) and causing store operations (see Col.1 line 56 – Col.2 line 2),

ii. Executes the fetched instructions out of program order (see Col.6 lines 4-16),

iii. Detects a load/store order violation wherein a load executes prior to a store on whose data the load depends (see Col.7 lines 28-45 and Col.8 line 41 - Col.9 line 30),

iv. Creates a store set comprising a store set identifier value that identifies the store of the load/store order violation, and wherein the store set identifier links the load to the store (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43),

v. Saves the store set to the store set identifier table (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43). Here, a "store set" corresponding to entries in the load buffer, the store buffer and the bus

queue is created upon detecting of a load/store order violation by making entries for the corresponding load and store instructions in their respective buffers (see Col.3 lines 25-40), as well as setting the invalid store flag in the store buffer (see Col.11 lines 1-41) and the inhibit load flag in the bus queue (see Col.12 lines 3-22), with the entries in the buffers being indexed by the sequence number and source/destination addresses of the instructions (see Col.12 lines 26-43).

vi. Determines whether the store is poisoned by a previously poisoned instruction (see Col.11 lines 13-41). Here, it is determined if there have been more than one store instructions with invalid (poison) flags, which causes the prior load instructions to be replied (see Col.11 lines 26-31). Thus, the current store instruction has been poisoned (invalidated) by a previously poisoned (invalidated) instruction.

vii. If the store is poisoned, sets a poison value that indicates through a store set dependence that the store is poisoned (see Col.11 lines 13-41). Here, the store invalid flag (510 of Fig.5) acts as a poison value (see Col.10 lines 54-59 and Col.11 lines 22-41).

viii. Re-processes said load if said poison value associated with said store indicates through the store set dependence that the store has been poisoned (see Col.11 lines 13-41); and

ix. Applies said poison value through the store set dependence to subsequent load/store order violation occurrences (see column 11, lines 13-41).

11. Claims 1 and 19 are nearly identical to claim 10. Claim 1 lacks the hardware structure of claim 10, and claim 19 lacks the input device of claim 10. However, both claims 1 and 19 encompass the same scope as claim 10. Therefore, claims 1 and 19 are rejected for the same reasons as claim 10.

12. Regarding claims 2, 11 and 20, taking claim 11 as exemplary, Merchant has taught the system of claim 10, wherein said poison value comprises a bit in a table (see Col.10 lines 54-59 and Col.11 lines 22-41).

13. Claims 2 and 20 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Therefore, claims 2 and 20 are rejected for the same reasons as claim 11.

14. Regarding claims 3, 12 and 21, taking claim 12 as exemplary, Merchant has taught the system of claim 10, wherein the store set includes a pointer that points to the poison value (see Col.12 lines 26-43). Here, since there is a pointer to a store instruction (destination address) that is contained in the store set tables, and the poison value is directly associated with the store instruction (see Fig.5 and Col.10 lines 54-59), there is a pointer to the poison value associated with that store instruction.

15. Claims 3 and 21 are nearly identical to claim 12, differing in their parent claims, but encompassing the same scope as claim 12. Therefore, claims 3 and 21 are rejected for the same reasons as claim 12.

16. Regarding claims 4, 13 and 22, taking claim 13 as exemplary, Merchant has taught the system of claim 10, wherein said store set includes a pair of tables which are used to identify said store instruction (see Col.11 lines 22-41 and Col.12 lines 26-43). Here, entries in the load buffer,

the memory ordering buffer, and the load buffer are all used in identifying a invalid store instruction.

17. Claims 4 and 22 are nearly identical to claim 13, differing in their parent claims, but encompassing the same scope as claim 13. Therefore, claims 4 and 22 are rejected for the same reasons as claim 13.

18. Regarding claims 5, 14 and 23, taking claim 14 as exemplary, Merchant has taught the system of claim 13, wherein said microprocessor clears said poison value when said store is no longer poisoned (see Col.3 lines 28-39).

19. Claims 5 and 23 are nearly identical to claim 14, differing in their parent claims, but encompassing the same scope as claim 14. Therefore, claims 5 and 23 are rejected for the same reasons as claim 14.

20. Regarding claim 24, Merchant has taught a computer system, comprising:

a. A fetch stage which fetches instructions including a store instruction (store) and a load instruction (load) that target a common memory location (see Col.3 line 54 – Col.4 line 8),

b. A store set identifier table coupled to said fetch stage (see column 6, lines 4-16 and 40-49 and Figures 2 and 3) that comprises a store set associated with said load, wherein said store set comprises a store set identifier that identifies said store of a load/store violation (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43); and

c. Logic coupled to said fetch stage and said store set identifier table (see column 6, line 65 to column 7, line 2), said logic

i. Determines if the data to be written by said store is stale (see Col.7 lines 28-45 and Col.8 line 41 - Col.9 line 30),

ii. If said data is stale, sets a value associated with said store (see Col.11 lines 13-41) and re-processes said load to execute after said data is no longer stale (see Col.11 lines 13-41). Here, the store invalid flag (510 of Fig.5) acts as a poison value (see Col.10 lines 54-59 and Col.11 lines 22-41).

iii. Establishes said store set for said load to include said store, and saves said value associated with said store in said store set identifier table (see Col.3 lines 25-40, Col.11 lines 1-41 and Col.12 lines 3-22, 26-43). Here, a "store set" corresponding to entries in the load buffer, the store buffer and the bus queue is created upon detecting of a load/store order violation by making entries for the corresponding load and store instructions in their respective buffers (see Col.3 lines 25-40), as well as setting the invalid store flag in the store buffer (see Col.11 lines 1-41) and the inhibit load flag in the bus queue (see Col.12 lines 3-22), with the entries in the buffers being indexed by the sequence number and source/destination addresses of the instructions (see Col.12 lines 26-43).

21. Regarding claim 26, Merchant has taught the system of claim 24, wherein said microprocessor uses said store set to access said value (see Col.12 line 62 – Col.13 line 10). Here, the processor has to access the memory order buffer and store buffer and the load buffer, which are the tables used in the store set, in order to check for an entry in the store buffer that is both older than a load instruction and has its invalid (poison) flag set.

22. Regarding claim 27, Merchant has taught the system of claim 24, wherein said value comprises a poison bit (see Col.10 lines 54-59 and Col.11 lines 22-41).

Response to Arguments

23. Examiner withdraws the claim objection to claim 14 in favor of the amended claim.

24. Applicant's arguments filed 15 November 2004 have been fully considered but they are not persuasive.

25. Applicant argues in essence on pages 7-9 in regards to claims 1, 10 and 19

> Merchant does not teach or even suggest a system comprising a microprocessor that creates and saves a "store set," in particular a store set that comprises a store set identifier value that identifies the store and that links the load to the store. Merchant also does not teach or suggest a system with a microprocessor that reprocesses the load based on a poison value that indicates through the store set that the store set is poisoned, or that reapplies the poison value through the store set to subsequent load/store order violation occurrences.

26. This has not been found persuasive. Merchant does teach a "store set" that identifies the store and links a load to the store. Merchant's memory ordering buffer (column 6, lines 4-16 and 40-49 and Figures 2 and 3) is a store set. It indicates the address of store and load instructions and provides control information about each instruction. For store instructions, it indicates whether the store is valid or not (column 10, lines 47-59 and Figure 5). If the store is not valid, subsequent loads, which have a greater sequence number, are re-executed, along with the store, until the store is valid which in turn assures that the load is valid (column 11, lines 13-41). The load instruction is linked to the store instruction via the sequence number, which indicates

whether the load is before or after the store, and the address, which indicates whether the store and load access the same location (column 9, lines 21-52). Please see the rejection above for the full rejection of claims 1, 10, and 19.

27. Applicant argues in essence on page 9 in regards to claim 24

> As amended, claim 24 is directed to a microprocessor comprising a store set identifier table that comprises a store set associated with said load, wherein said store set comprises a store set identifier that identifies said store of a load/store violation...also comprises logic that establishes said store set for said load to include said store, and saves said value associated with said store in said store set identifier table. Merchant does not teach or suggest a microprocessor comprising the limitation described...

28. This has not been found persuasive. Merchant has taught a "store set" table called a memory ordering buffer (column 6, lines 4-16 and 40-49 and Figures 2 and 3). The store buffer has a saved valid bit that indicates whether the store was valid or not (column 10, lines 47-59 and Figure 5). If the store is not valid, subsequent loads, which have a greater sequence number, are re-executed, along with the store, until the store is valid which in turn assures that the load is valid (column 11, lines 13-41). The load instruction is linked to the store instruction via the sequence number, which indicates whether the load is before or after the store, and the address, which indicates whether the store and load access the same location (column 9, lines 21-52). Please see the rejection above for the full rejection of claim 24.

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
24 January 2005

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100